GENERAL DESCRIPTION

The EM78P154A/B is an 8-bit microprocessor with low-power, high speed CMOS technology. There are 0.64Kx13 bits Electrical One Time Programmable Read Only Memory (OTP-ROM) within it. It provides 13 Security bits and 6 One-time Programmable Option bits to protect the OTP memory code from any external access as well as the user's options.

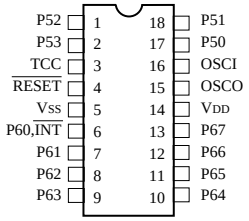
The OTP ROM will be incorporated into EM78P154A/B 8-bit microcontroller instead of it's original memory. The user's development program can be easily programmed into or verify from this OTP memory by using EMC OTP WRITER.

FEATURES

- Operating voltage range : 2.5V ~ 6.5V
- Available in temperature range:
- Operation Speed : DC ~ 36 MHz
- Low power consumption :
  * <2mA, at 5V/4MHz
  * 15μA typical, at 3V/32KHz
  * 1μA typical, at sleep
- 0.64K x 13 Electrical Programmable Read Only Memory (OTP-ROM)
- One Security Register is provided to protect the OTP memory code and to define user's ID code.
- One Configuration Register is provided to meet the user's options.
- 14 special function registers.
- 48 x 8 on chip RAM.
- 2 bi-directional tri-state I/O ports (12 I/O pins).
- 5 level stack for subroutine nesting.
- 8-bit real time clock/counter (TCC) with selective signal sources and trigger edges, and with overflow interrupt.
- Programmable free running on-chip watchdog timer.
- Two R-option pin.
- Power down mode.
- Input port change interrupt (wake-up), and external interrupt available.
- 99.9% single instruction cycle commands.
- 18 pin DIP, 18 pin SOIC, 20 pin SSOP.
- Power on voltage detector.
  - EM78P154A : enabled
  - EM78P154B : disabled
- Function compatiable with EM78156 except OTP memory inside.

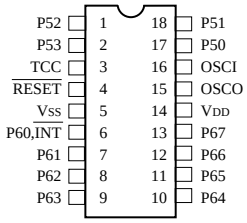
PIN ASSIGNMENTS

EM78P154AP/BP



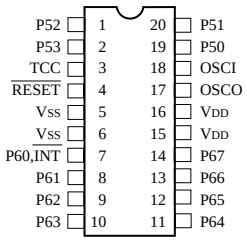
DIP

EM78P154AM/BM



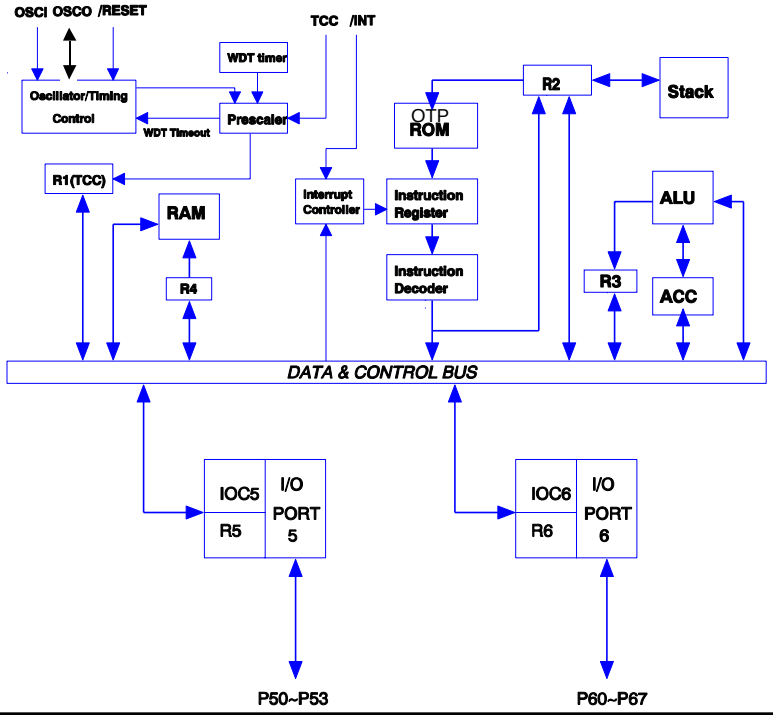
SOIC

EM78P154AS/BS



SSOP

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

Symbol	I/O	Function
OSCI	I	XTAL type : Crystal input terminal or external clock input pin. RC type: RC oscillator input pin.
OSCO	I/O	XTAL type: output terminal for crystal oscillator or external clock input pin. RC type: clock output with a period of one instruction cycle is put on this pin.
TCC	I	Real time clock/counter, Schmitt trigger input pin. Must be tied to V_{DD} or V_{SS} if not in use.
$\overline{\text{RESET}}$	I	Schmitt trigger input pin. If this pin remains logic low, the controller is reset.
P50~P53	I/O	P50~P53 are bi-directional I/O ports. P50 and P51 are also the R-option pins. P50~P52 can be pulled-down by software control.

Symbol	I/O	Function
P60~P67	I/O	P60~P67 are bi-directional I/O ports. They can be pulled-high internally by software control and can have open-drain output by software control. In addition, P60~P63 can be pulled-down by software control.
$\overline{INT}$	I	Falling edge triggered, external interrupt input pin. It is the secondary function of P60.
V_{DD}	-	Power supply pin.
V_{SS}	-	Ground pin.

FUNCTION DESCRIPTIONS

Operational Registers

R0 (Indirect Addressing Register)

- R0 is not a physically implemented register. It is useful as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

R1 (TCC)

- Increased by an external signal edge applied to TCC pin, or by the instruction cycle clock.
- Written and read by the program as any other register.

R2 (Program Counter) & Stack

- Generates 0.64K x 13 on-chip OTP ROM addresses to the relative programming instruction codes. One program page is 0.64K words long.
- R2 is set all "0"s upon s RESET condition.
- "JMP" instruction allows the direct loading of the lower 10 program counter bits. Thus, "JMP" allows jump to any location on one page.
- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be any location on one page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.
- "ADD R2,A" allows a relative address be added to the current PC, and contents of the ninth and tenth bits of PC are cleared.
- "MOV R2,A" allows the loading of an address from the "A" register to the lower 8 bits of PC, and the ninth and tenth bits of PC are cleared.
- Any instruction which writes to R2 (e.g. "ADD R2,A", "MOV R2,A", "BC R2,6",....) will cause the ninth and tenth bits (A8~A9) of PC to be cleared. Thus, the computed jump is limited to the first 256 locations of any program page.
- All instructions are single instruction cycle except that the instructions which write to R2 need one more instruction cycle.

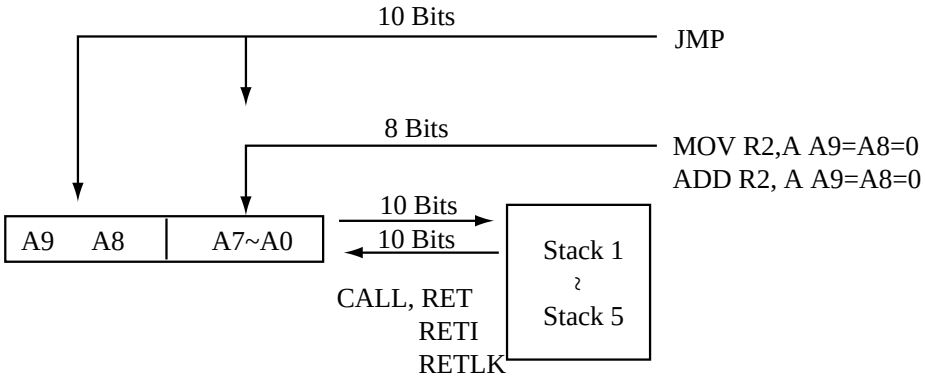


Fig. 3 Program counter organization

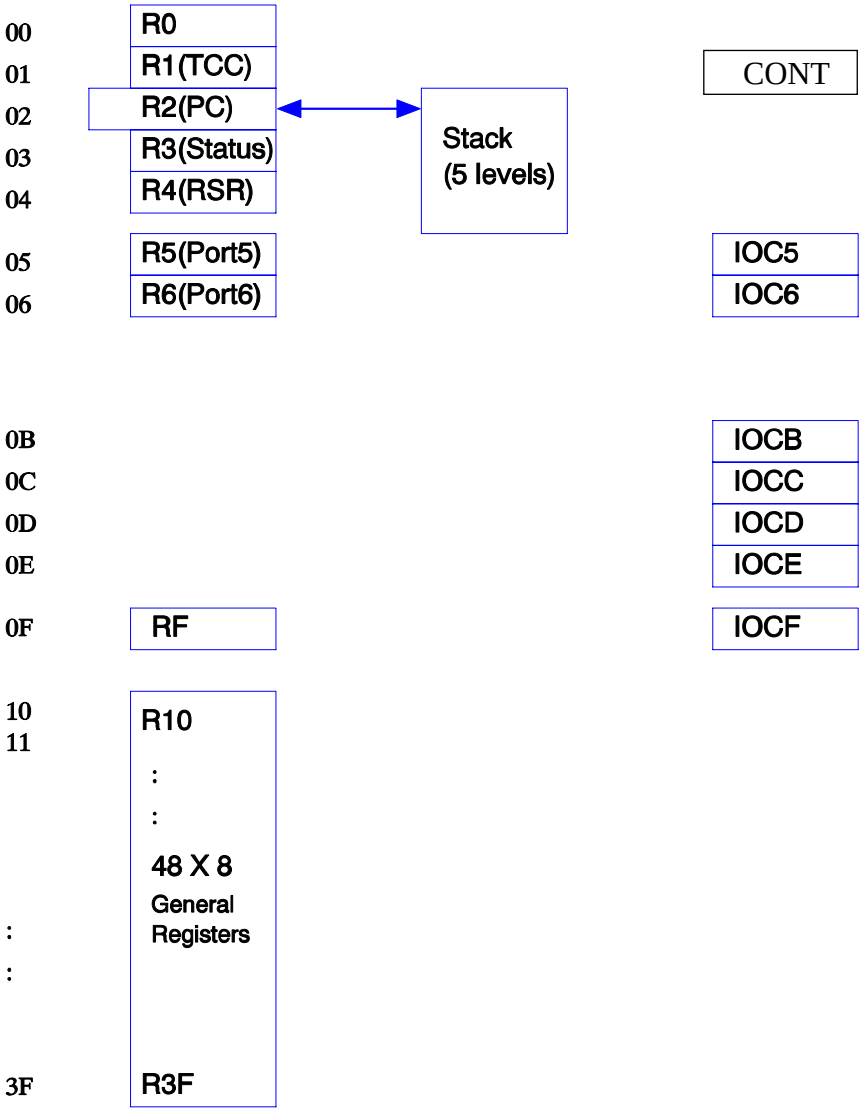


Fig. 4 Data memory configuration

R3 (Status Register)

7	6	5	4	3	2	1	0
GP2	GP1	GP0	T	P	Z	DC	C

Bit 0 (C) Carry flag
Bit 1 (DC) Auxiliary carry flag
Bit 2 (Z) Zero flag. Set to "1" if the result of an arithmetic or logic operation is zero.
Bit 3 (P) Power down bit. Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.
Bit 4 (T) Time-out bit. Set to 1 by the "SLEP" and "WDTC" command, or during power up and reset to 0 by WDT timeout.
Bit 5~7 (GP0~2) General purpose read/write bit.

R4 (RAM Select Register)

- Bits 0 ~ 5 are used to select registers (address: 00~06, 0F~3F) in the indirect addressing mode.
- If no indirect addressing is used, the RSR can be used as an 6-bit wide general purpose read/write register.
- Bits 6 ~ 7 are general register.
- See the configuration of the data memory in Fig. 4.

R5 ~ R6 (Port 5 ~ Port 6)

- R5 and R6 are I/O registers.
- Only low order 4 bits are used in R5.

RF (Interrupt Status Register)

7	6	5	4	3	2	1	0
-	-	-	-	-	EXIF	ICIF	TCIF

• "1" means interrupt request, "0" means non-interrupt

Bit 0 (TCIF) TCC timer overflow interrupt flag. Set when TCC timer overflows, reset in software.
Bit 1 (ICIF) Port 6 input change interrupt flag. Set when Port 6 input changes, reset in software.
Bit 2 (EXIF) External interrupt flag. Set by falling edge on /INT pin, reset in software.
Bits 3 ~ 7 Not used.

- RF can be cleared by instruction and cannot be set by instruction.
- IOCF is the interrupt mask register.
- Note that reading RF by instruction will get the result of "logic AND" of RF and IOCF.

R10 ~ R3F

- R10 ~ R3F are the 48x8 general purpose registers.

Special Purpose Registers

A (Accumulator)

- Internal data transfer, or instruction operand holding
- It's not an addressable register.

CONT (Control Register)

7	6	5	4	3	2	1	0
-	INT	TS	TE	PAB	PSR2	PSR1	PSR0

Bit 0 (PSR0) TCC/WDT prescaler bits.
ž
Bit 2 (PSR2)

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 3 (PAB) Prescaler assignment bit.
0: TCC
1: WDT
Bit 4 (TE) TCC signal edge
0: increment from low to high transition on TCC pin
1: increment from high to low transition on TCC pin
Bit 5 (TS) TCC signal source
0: internal instruction cycle clock
1: transition on TCC pin
Bit 6 (INT) INT enable flag
0: interrupt masked by DISI or hardware interrupt
1: interrupt enabled by ENI/RETI instructions
Bit 7 Not used.

- CONT register is readable and writable.

IOC5 ~ IOC6 (I/O Port Control Register)

- "1" put the relative I/O pin into high impedance, while "0" put the relative I/O pin as output.
- Low order 4 bits are used in IOC5.
- IOC5 and IOC6 registers are readable and writable.

IOCB (Pull-down Control Register)

7	6	5	4	3	2	1	0
/PD7	/PD6	/PD5	/PD4	-	/PD2	/PD1	/PD0

Bit 0 (/PD0) Control bit used to enable the pull-down of P50 pin.
0: Enable internal pull-down
1: Disable internal pull-down
Bit 1 (/PD1) Control bit used to enable the pull-down of P51 pin.
Bit 2 (/PD2) Control bit used to enable the pull-down of P52 pin.
Bit 3 Not used.
Bit 4 (/PD4) Control bit used to enable the pull-down of P60 pin.
Bit 5 (/PD5) Control bit used to enable the pull-down of P61 pin.
Bit 6 (/PD6) Control bit used to enable the pull-down of P62 pin.
Bit 7 (/PD7) Control bit used to enable the pull-down of P63 pin.

• IOCB Register is readable and writable.

IOCC (Open-drain Control Register)

7	6	5	4	3	2	1	0
OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0

Bit 0 (OD0) Control bit used to enable the open-drain of P60 pin.
0: Disable open-drain output
1: Enable open-drain output
Bit 1 (OD1) Control bit used to enable the open-drain of P61 pin.
Bit 2 (OD2) Control bit used to enable the open-drain of P62 pin.
Bit 3 (OD3) Control bit used to enable the open-drain of P63 pin.
Bit 4 (OD4) Control bit used to enable the open-drain of P64 pin.
Bit 5 (OD5) Control bit used to enable the open-drain of P65 pin.
Bit 6 (OD6) Control bit used to enable the open-drain of P66 pin.
Bit 7 (OD7) Control bit used to enable the open-drain of P67 pin.

• IOCC Register is readable and writable.

IOCD (Pull-high Control Register)

7	6	5	4	3	2	1	0
/PH7	/PH6	/PH5	/PH4	/PH3	/PH2	/PH1	/PH0

Bit 0 (/PH0) Control bit used to enable the pull-high of P60 pin.
0: Enable internal pull-high
1: Disable internal pull-high
Bit 1 (/PH1) Control bit used to enable the pull-high of P61 pin.
Bit 2 (/PH2) Control bit used to enable the pull-high of P62 pin.
Bit 3 (/PH3) Control bit used to enable the pull-high of P63 pin.
Bit 4 (/PH4) Control bit used to enable the pull-high of P64 pin.
Bit 5 (/PH5) Control bit used to enable the pull-high of P65 pin.
Bit 6 (/PH6) Control bit used to enable the pull-high of P66 pin.
Bit 7 (/PH7) Control bit used to enable the pull-high of P67 pin.

• IOCD Register is readable and writable.

IOCE (WDT Control Register)

7	6	5	4	3	2	1	0
WDTE	EIS	-	ROC	-	-	-	-

Bit 7 (WDTE) Control bit used to enable Watchdog timer.
0: Disable WDT
1: Enable WDT
WDTE bit is readable and writable.

Bit 6 (EIS) Control bit used to select the function of P60(/INT) pin.
0: P60, bidirectional I/O pin.
1: /INT, external interrupt input pin. In this case, the I/O control bit of P60 (bit 0 of IOC6) must be set to "1".
When EIS is "0", the path of /INT is masked. When EIS is "1", the status of /INT pin can also be read by Port 6(R6). Refer to Fig. 7(a). EIS bit is readable and writable.

Bit 4 (ROC) ROC is used for the R-option. Setting ROC to "1" will enable the status of R-option pins (P50~P51) to be read by the controller. Clearing ROC will disable the R-option function. If the R-option function is used, the user must connect the P51 pin or/and P50 pin to VSS by a 430KΩ external resistir (Rex). If Rex is connected/disconnected, the status of P50(P51) will be read as "0"/"1" when ROC is set to "1". Refer to Fig. 8. ROC bit is readable and writable.

Bits 0 ~ 3, 5 Not used.

IOCF (Interrupt Mask Register)

7	6	5	4	3	2	1	0
-	-	-	-	-	EXIE	ICIE	TCIE

Bit 0 (TCIE) TCIF interrupt enable bit.
0: disable TCIF interrupt
1: enable TCIF interrupt

Bit 1 (ICIE) ICIF interrupt enable bit.
0: disable ICIF interrupt
1: enable ICIF interrupt

Bit 2 (EXIE) EXIF interrupt enable bit.
0: disable EXIF interrupt
1: enable EXIF interrupt

Bits 3 ~ 7 Not used.

- Individual interrupt is enabled by setting its associated control bit in IOCF to "1".
- Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. Refer to Fig.10.
- IOCF register is readable and writable.

TCC/WDT & Prescaler

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for the TCC only or WDT only at the same time and the PAB bit of CONT register is used to determine the prescaler assignment. The PSR0~PSR2 bits determine the prescale ratio. Fig. 5 depicts the circuit diagram of TCC/WDT.

- R1(TCC) is an 8-bit timer/counter. The clock source of TCC can be internal clock or external clock input (edge selectable from TCC pin). TCC will increase by 1 every instruction cycle (without prescaler). The prescaler will be cleared by instructions which write to TCC each time, when assigned to TCC mode.
- The watchdog timer is a free running on-chip RC oscillator. The WDT will keep running even the oscillator driver has been turned off (i.e. in sleep mode). During the normal operation or the sleep mode, WDT time-out

(if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during the normal mode by software programming. Refer to WDTE bit IOCE register. With no presacler, the WDT time-out period is approximately 18 ms. The WDT and prescaler, when assigned to WDT mode, will be cleared by the WDTC and CLEP instructions.

I/O Ports

The I/O registers, Port 5~Port 6, are bi-directional tri-state I/O ports. Port 6 can be pulled-high internally by software control. In addition, Port 6 can also have open-drain output by software control. There are input change interrupt (or wake-up) function on Port 6. P50~P52 and P60~P63 pins can be pulled-down by sodtware control. Each I/O pins can be defined as "input" or "output" pins by the I/O control register (IOC5~IOC6) under program control. P50~P51 are the R-option pins which are enabled by software. While R-option function is used, P50~P51 are recommed as input pins. If external resistor is connected to P50(P51) for R-option function, the current consumption should be noticed in the applications that low power are concerned.

The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5 and Port 6 are shown in Fig. 6 and Fig. 7(a), (b) respectively.

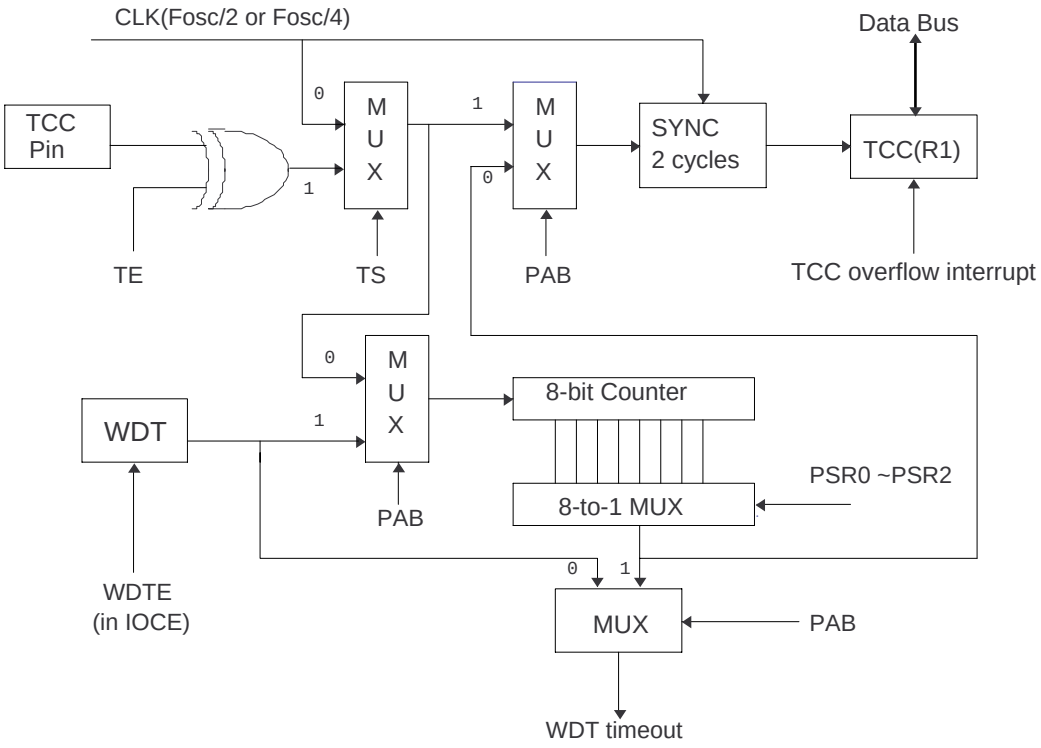
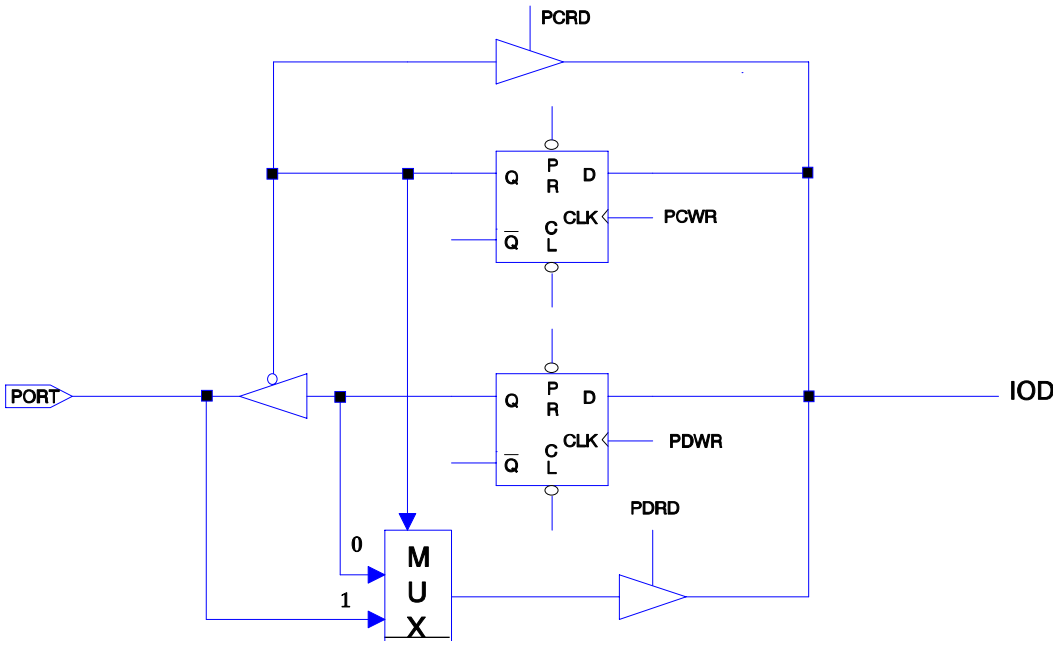
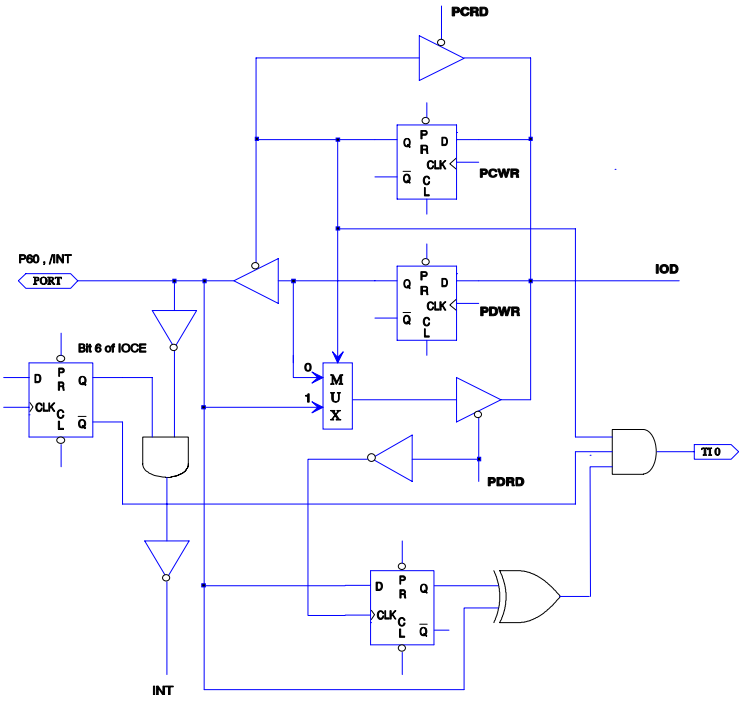


Fig. 5 Block diagram of TCC and WDT



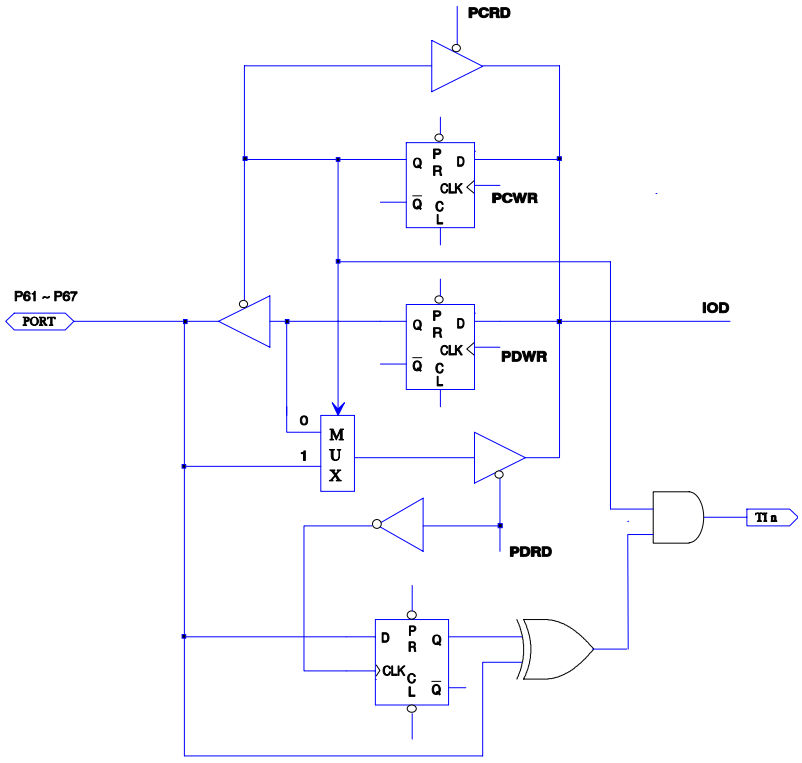
*Pull-down is not shown in the figure.

Fig. 6 The circuit of I/O port and I/O control register for Port 5



*Pull-high (down), Open-drain are not shown in the figure.

Fig. 7(a) The circuit of I/O port and I/O control register for P60(/INT)



*Pull-high (down), Open-drain are not shown in the figure.

Fig. 7(b) The circuit of I/O port and I/O control register for P61~P67

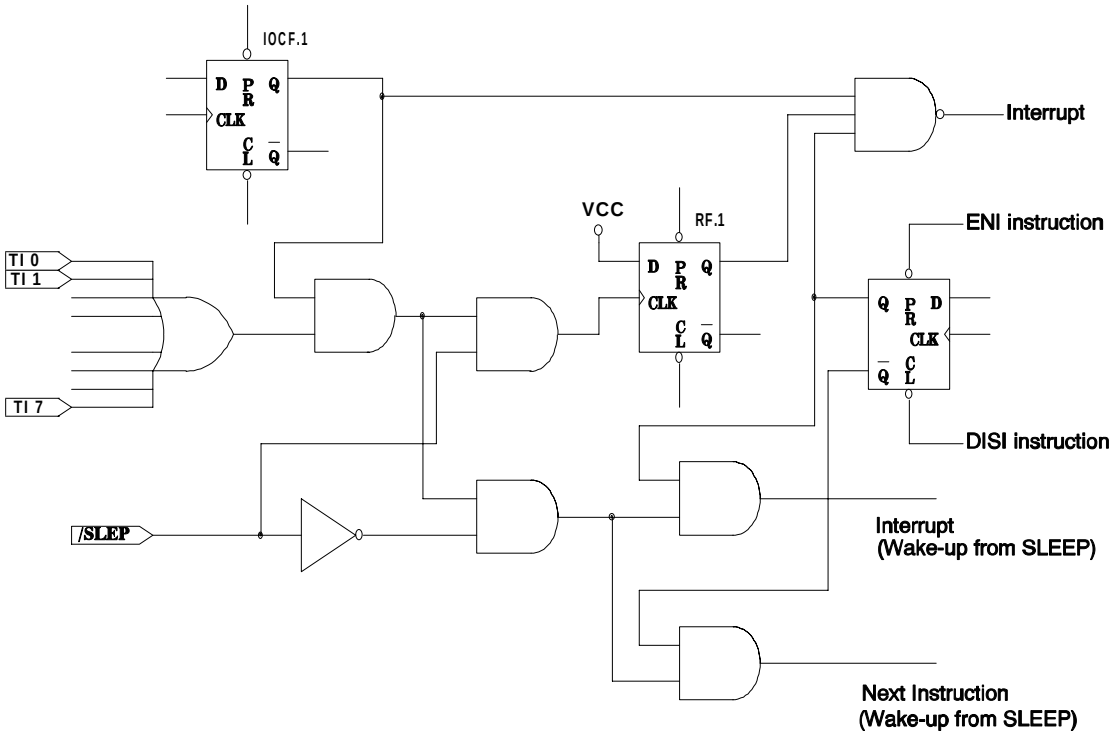
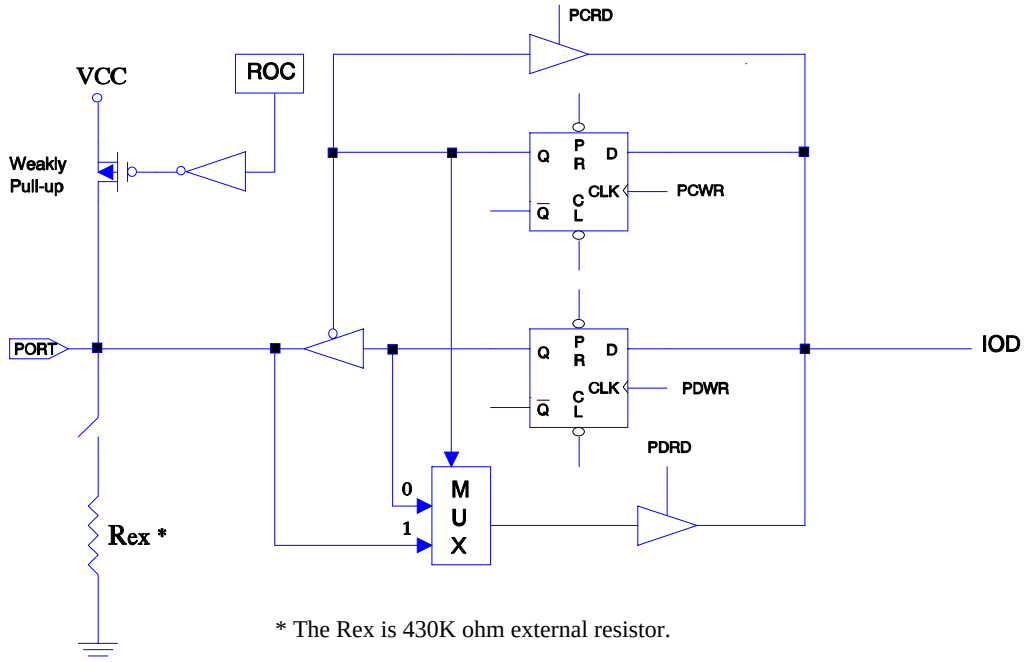


Fig. 7(c) Block diagram of I/O Port 6 with input change interrupt/wake-up

Usage of Port 6 input change Wake-up/Interrupt	
(I) Wake-up from Port 6 input change (a) Before SLEEP 1. Disable WDT 2. Read I/O Port 6 (MOV R6,R6) 3. Execute "ENI" or "DISI" 4. Enable interrupt (Set IOCF.1) 5. execute “SLEP” instruction (b) After Wake-up 1. IF "ENI" → Interrupt vector (008H) 2. IF "DISI" → Next instruction	(II) Port 6 input change Interrupt 1. Read I/O Port 6 (MOV R6,R6) 2. Execute "ENI" 3. Enable interrupt (Set IOCF.1) 4. IF Port 6 change (interrupt) → Interrupt vector (008H)

Fig. 7(d) Usage of Port 6 input change wake-up/interrupt function



* The Rex is 430K ohm external resistor.

Fig. 8 The circuit of I/O port with R-option (P50,P51)

RESET and Wake-up

The RESET can be caused by
(1) Power on reset, or Voltage detector
(2) $\overline{\text{RESET}}$ pin input "low", or
(3) WDT timeout (if enabled).

Note that only Power on reset, or only Voltage detector in Case(1) is enabled in the system by CODE option bit . Refer to Fig. 9. The device will be kept in a RESET condition for a period of approx. 18ms (one oscillator start-up timer period) after the reset is detected. Once the RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).

- The Watchdog timer and prescaler are cleared.
- When power on, the upper 3 bits of R3 are cleared.
- The CONT register is set to all "1" except the bit 6 (INT flag).
- IOCB register is set to all "1".
- IOCC register is cleared.
- IOCD register is set to all "1".
- Bit 7 of IOCE register is set to "1" and Bits 4 and 6 of IOCE are cleared.
- Bits 0~2 of RF and bits 0~2 of IOCF register are cleared.

The sleep mode (power down mode) can be entered by executing the SLEP instruction. While entering sleep mode, the WDT (if enabled) is cleared but keeping running. The controller can be awakened by
(1) external reset input on $\overline{\text{RESET}}$ pin,
(2) WDT time-out (if enabled), or
(3) Port 6 input change (if enabled).

The two former cases will cause the controller reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). The last case is considered a continuation of program execution and the global interrupt (ENI or DISI being executed) decides whether or not the controller branches to the interrupt vector following wake-up. If ENI instruction is executed before "SLEP", the instruction to be fetched is from 008H after wake-up. If DISI instruction is executed before "SLEP", the instruction to be fetched is next instruction (the one after "SLEP" instruction) after wake-up.

Only one of the cases 2 and 3 can be enabled before entering SLEEP Mode. That is,
[a] if Port 6 input change interrupt is enabled before "SLEP" instruction, the WDT must be disabled. Hence, the controller can be awakened only by case 1 or 3.
[b] if WDT is enabled before "SLEP" instruction, Port 6 input change interrupt must be disabled. Hence, the controller can be awakened only by case 1 or 2. Refer to interrupt section.

If Port 6 input change interrupt is used to wake-up the controller (the case [a]), the following instructions must be executed before "SLEP".

```
MOV A, xx000110b      ; Select internal TCC clock
CONTW
CLR R1                ; Clear TCC and prescaler
MOV A, xxxx1110b      ; Select WDT and prescaler
CONTW
WDTC                  ; Clear WDT and prescaler
MOV A, 0xxxxxxxb      ; Disable WDT
IOW RE
MOV R6, R6            ; Read Port 6
MOV A, 00000x1xb      ; Enable Port 6 input interrupt
IOW RF
ENI (or DISI)         ; Enable (or disable) global interrupt
SLEP                  ; Sleep
NOP
```

One caution should be noted is that after wake-up from SLEEP Mode, the WDT is enabled. The WDT operation (being enabled or disabled) should be appropriately controlled by software after wake-up from "SLEP".

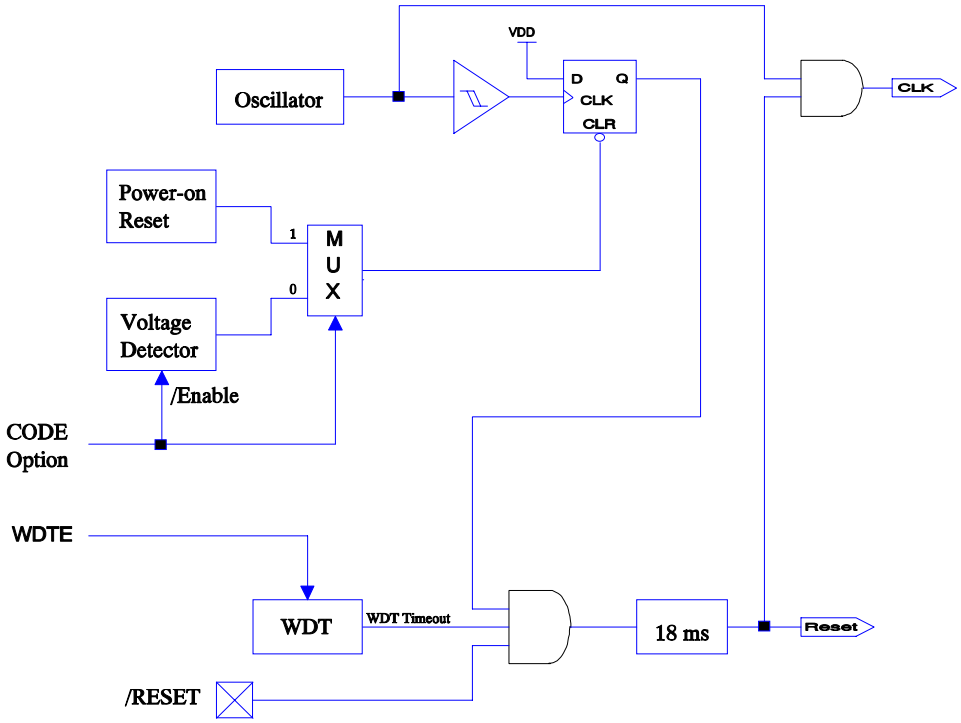


Fig. 9 Block diagram of Reset of controller

Interrupt

The EM78P154 has interrupts which are falling edge triggered, as listed in following:
(1) TCC timer overflow interrupt
(2) Port 6 input change interrupt
(3) External interrupt (P60/$\overline{INT}$ pin).

Before enabling Port 6 input change interrupt, reading Port 6 (e.g. MOV R6,R6) is necessary. Each pin of Port 6 has the feature of interrupt on change. Any pin configured as output is excluded from this feature. The Port 6 interrupt can wake up the controller from SLEEP Mode if interrupt is enabled prior to going into SLEEP Mode by executing the "SLEP" instruction. When wake-up, the controller will continue to execute program in-line if global interrupt is disabled or branch to the interrupt vector 008H if global interrupt is enabled.

RF is the interrupt status register which records the interrupt request in flag bit. IOCF is the interrupt mask register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) generated, will cause the next instruction to be fetched from address 008H. Once in the interrupt service routine the source of the interrupt can be determined by polling the flag bits in the RF register. The interrupt flag bit must be cleared in software before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF) is set regardless of the status of its mask bit or the execution of ENI instruction. Note that reading RF will get the output of logic AND of RF and IOCF. Refer to Fig. 10. The RETI instruction exits interrupt routine and enables the global interrupt (execution of ENI instruction).

When an interrupt is generated by INT instruction (when enabled), causes the next instruction to be fetched from address 001H. The locations of address 002H ~ 007H are reserved for special purpose (must be "NOP"s).

Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A'', "ADD R2,A'', or instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS (BC) R2,b", "CLR R2", ...). In this case, the execution takes two instruction cycles.

Under some condition, if the specification of the instruction cycle is not suitable for some applications, they can be modified as follows:

(A) one instruction cycle consists of 4 oscillator periods.

(B)"JMP", "CALL", "RET", "RETL", "RETI", or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") is tesed to be true are executed within two instruction cycles. The instructions that write to the program counter also take two instruction cycles.

The Case(A) is selected by the CODE Option bit (CLKS). One instruction cycle consists of two oscillator clocks if CLKS bit is low, and consists of four oscillator clocks if CLKS bit is high. The Case(B) is selected by the CODE Option bit (CYES). The execution of those instructions listed in Case (B) takes one instruction cycle if CYES bit is low, and takes two instruction cycles if CYES bit is high. Case(A) and Case(B) are independent options, that is, they can be selected individually. Note that once 4 oscillator periods within one instruction cycle is selected in Case(A), the internal clock source to TCC is CLK=Fosc/4 instead of Fosc/ 2 that is shown in Fig. 5.

In addition, the instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operates on I/O register.

The symbol "R'' represents a register designator which specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction. "b'' represents a bit field designator which selects the number of the bit, located in the register "R'', affected by the operation.

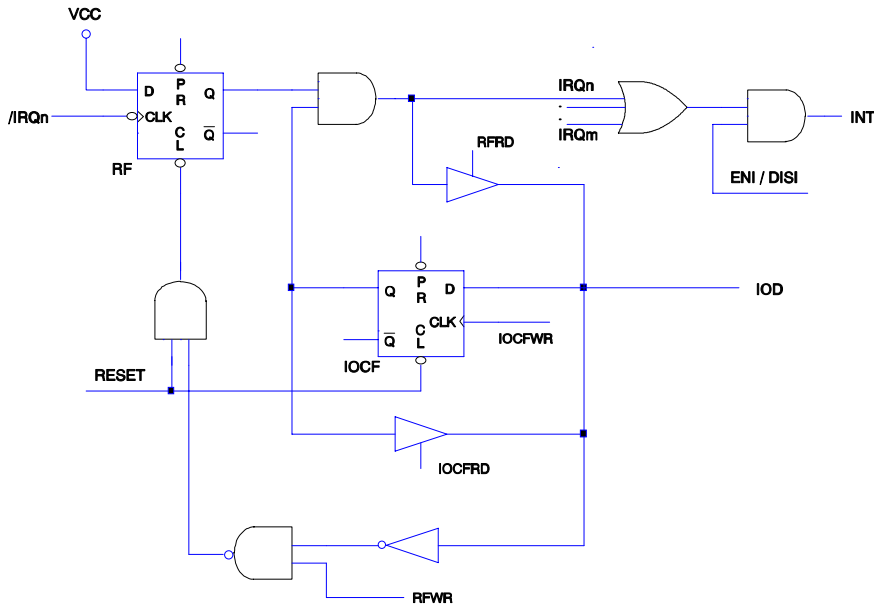


Fig. 10 Interrupt input circuit

"k'' represents an 8 or 10-bit constant or literal value.

INSTRUCTION BINARY	HEX	HNEMONIC	OPERATION	STATUS AFFECTED
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None <Note1>
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None <Note1>
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C,DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C,DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z,C,DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z,C,DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1) R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1) R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1) R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1) R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7) R(4-7) → A(0-3)	None

INSTRUCTION BINARY	HEX	HNEMONIC	OPERATION	STATUS AFFECTED
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None <Note2>
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None <Note3>
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC
1 1110 0000 0001	1E01	INT	PC+1 → [SP], 001H → PC	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC

<Note 1> This instruction can operate on IOC5~IOC6, IOCB~IOCF only.
<Note 2> This instruction is not recommended to operate on RF.
<Note 3> This instruction cannot operate on RF.

CODE Option Register

The EM78P154 has one option register which is not part of the normal program memory. The option register cannot be accessed during normal program execution.

12	11	10	9	8	7	6~0
MS	ENWDTB	CLKS	CYES	HLF	HLP	------

Bit 12 (MS): Oscillator type selection
0: RC type
1: XTAL type
Bit 11 (ENWDTB): Watchdog timer enable
0: Enable
1: Disable
Bit 10 (CLKS): Clocks of each instruction cycle
0: Two clocks
1: Four clocks
Bit 9 (CYES): Cycles of conditional skip instruction
0: One cycle
1: Two cycles
Bit 8 (HLF): XTAL frequency selection.
0: Low frequency (32.768KHz)
1: High frequency
This bit is useful only when Bit 12 (MS) is "1". When MS is "0", HLF must be "0".
Bit 7 (HLP): Power consumption selection.(Ref P19)
0: Low power
1: High power

Bit 6~0 : Not used. (default "00000001")

Security Mode ------ Security Register

The EM78P154 has one security register which is not part of the normal program memory. The security register cannot be accessed during normal program execution.

12	11~0
/PT	--------

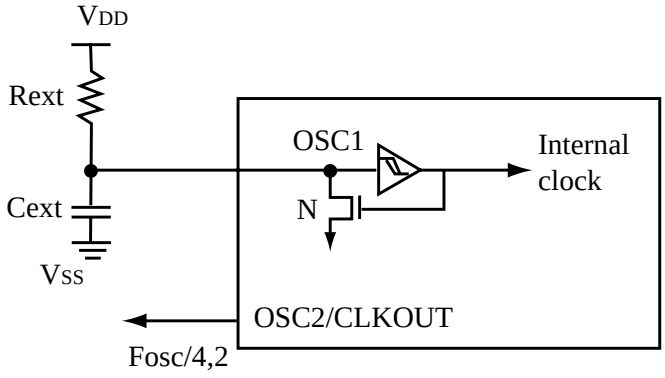
Bit 12 (/PT) : Protect bit
0: Protect enable
1: Protect disable
(User's program in OTP-ROM cannot be read through IO0~IO6)
Bit 11~0 : User's ID code.

Oscillator

The EM78P154A/B can be operated in there different oscillator options, three are RC type, low XTAL type, high XTAL type. The user can program three option bits (MS, HLF, HLP) to select one of these three modes.
If MS=0, HLF=0, RC type oscillator is chosed and the frequency is determined by external Rext, Cext which device can offer lots of cost saving in timing insensitive applications.
If MS=1, HLF=0, HLP=0, low XTAL type oscillator is chosed, in this case the oscillator is in low power and low frequency operation condition so the maxim frequency should not excess 4 MHz and you got the bonus of low current consumption.
If MS=1, HLF=1, HLP=1, high XTAL type oscillator is chosed, at this situation the oscillator is in high speed operation condition so the minum frequency should not less than 1MHz. Because in this mode the current consumption is large than low power mode which in low frequency operation or battery environment should take into consideration.

The typical operation speeds of Crystal are listed below :

Conditions	VDD (V)	Fxt max. (M)
One cycles with two clocks	2.5	3.58
	3	4
	5	12
	6.5	17
Two cycles with two clocks	2.5	3.84
	3	5
	5	15
	6	17
One cycles with four clocks	2.5	8
	3	10
	5	28
	6	33
Two cycles with foue clocks	2.5	9
	3	11
	5	31
	6	36



Cext	Rext	Average Fosc @ 5V, 25°C	Average Fosc @ 3V, 25°C
20pF	3.3k	3.20 MHz	2.47 MHz
	5.1k	2.22 MHz	1.83 MHz
	10k	1.28 MHz	1.14 MHz
	100k	150 KHz	143 KHz
100pF	3.3k	1.13 MHz	974 KHz
	5.1k	758 KHz	675 KHz
	10k	409 KHz	376 KHz
	100k	51 KHz	43.7 KHz
300pF	3.3k	472 KHz	420 KHz
	5.1k	310 KHz	283 KHz
	10k	165 KHz	153 KHz
	100k	17.5 KHz	17.0 KHz

* Measured on DIP packages.

In most case, the timing accuracy is not very important . So the "RC Oscillator" offers lots of cost savings. But the RC oscillator frequency is a function of the supply voltage, the resistor (Rext), capacitor (Cext) values and the operation temperature. In addition to this, the oscillator frequency will vary little from unit to unit due to process parameter variation.
We strongly suggest user should take into account the frequency variation due to tolerance of Rext, Cext values and the voltage temperature effect.
Besides, for more stable consideration, the Cext should not less than 20pF and Rext should not great than 1M Ohm. In such case the PCB trace capacitance, package lead frame capacitance and leakage current will become frequency insensitive.
If the Rext become smaller the frequency become faster, However when Rext value less the 1K Ohm there may occure unstable condition due to the NMOS can't discharge the capacitance's current correctly the user should pay attention on it.

Power on Voltage Detector

The EM78P154A internal built-in power on voltage detector whichs detect level is set at 1.8 voltage.
At some application you may find out your system would lost control after power on-off occured. In this circumstance we suggested strongly you should using the EM78P154A instead of EM78P154B.
No pains no gains, How ever using EM78P154A the internal power on voltage detector cost you 15 μA current consumption . So in some power consumption considerable application you should think about 15μA pain.

ABSOLUTE MAXIMUM RATINGS

Items	Sym.	Condition	Rating
Temperature under bias	T_{OPR}		0°C to 70°C
Storage temperature	T_{STR}		-65°C to 150°C
Input voltage	V_{IN}		-0.3V to +6.0V
Output voltage	V_O		-0.3V to +6.0V

DC ELECTRICAL CHARACTERISTIC (T_A=0°C ~ 70°C, V_{DD}=5.0V±5%, V_{SS}=0V)

Parameter	Sym.	Condition	Min.	Typ.	Max.	Unit
Supply Oscillator Crystal : VDD to 3V	Fxt	One Cycle with two clocks	DC		4.0	MHz
VDD to 5V			DC		12.0	MHz
RC : VDD to 5V	F_{RC}	R : 5.0KΩ , C : 39pf	F_{RC}±20%	602	F_{RC}±20%	KHz
Input Leakage Current for input pins	I_{IL1}	V_{IN} = V_{DD}, V_{SS}			±1	µA
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input High Threshold Voltage	V_{IHT}	$\overline{RESET}$, TCC	2.0			V
Input Low Threshold Voltage	V_{ILT}	$\overline{RESET}$, TCC			0.8	V
Clock Input High Voltage	V_{IHX}	OSCI	3.5			V
Clock Input Low Voltage	V_{ILX}	OSCI			1.5	V
Output High Voltage (Port 5,6)	V_{OH1}	I_{OH} = -10.0mA	2.4			V
Output Low Voltage (P50~P53,P60~P63,P66~P67)	V_{OL1}	I_{OL} = 7.0mA			0.4	V
Output Low Voltage (P64,P65)	V_{OL2}	I_{OL} = 10.0mA			0.4	V
Pull-high current	I_{PH}	Pull-high active, input pin at V_{SS}	-50	-100	-240	µA
Pull-down current	I_{PD}	Pull-down active, input pin at V_{DD}	25	50	120	µA
Power down current	I_{SB}	All input and I/O pins at V_{DD}, output pin floating, WDT enabled		1		µA
Operating supply current (V_{DD}=3V)	I_{CC1}	$\overline{RESET}$='High', Fosc=32KHz(Crystal type, CLKS="0"), output pin floating, input pins at V_{DD} , WDT disabled	15	15	30	µA
Operating supply current (V_{DD}=3V)	I_{CC2}	$\overline{RESET}$='High', Fosc=32KHz(Crystal type,CLKS="0"), output pin floating, input pins at V_{DD} , WDT enabled		20	35	µA
Operating supply current	I_{CC3}	$\overline{RESET}$='High', Fosc=4MHz (Crystal type,CLKS="0"), output pin floating			2	mA
Operating supply current	I_{CC4}	$\overline{RESET}$='High', Fosc=12MHz (Crystal type,CLKS="0"), output pin floating			4	mA

VOLTAGE DETECTOR ELECTRICAL CHARACTERISTIC (T_A = 25°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Detect voltage	Vdet	V_{DD} = 5V	1.6	1.8	2.0	V
Release voltage	Vrel	V_{DD} = 5V	Vdet x1.05			V
Current consumption	Iss	V_{DD} = 5V			20	μA
Operating voltage	Vop		0.7*		5.5	V
Temperature characteristic of Vdet	ΔVdet/ ΔT_A	0°C ≤T≤ 70°C			-2	mV/°C

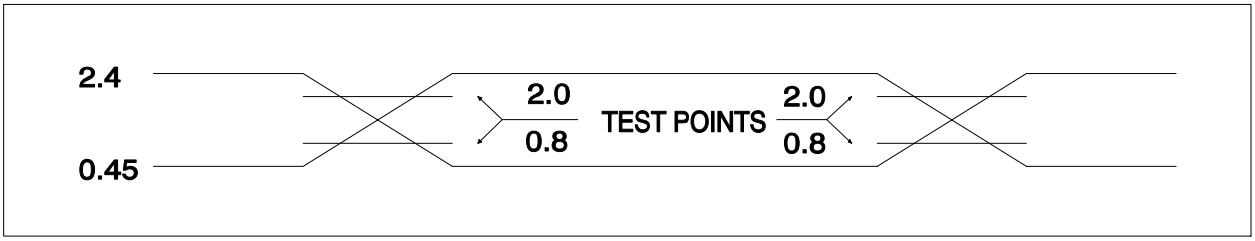
* When the voltage of V_{DD} rises between Vop=0.7V and Vdet, the output of voltage detector must be "Low".

AC ELECTRICAL CHARACTERISTICS (T_A=0°C ~ 70°C, V_{DD}=5.0V±5%, V_{SS}=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input CLK duty cycle	Dclk		45	50	55	%
Instruction cycle time (CLKS="0")	Tins	XTAL Type	125		DC	ns
		RC Type	500		DC	ns
TCC input period	Ttcc	Note 1	(Tins+20)/N			ns
Device reset hold time	Tdr	Ta = 25°C		18		ms
Watchdog timer period	Twdt	Ta = 25°C		18		ms
Input pin setup time	Tset			0		ns
Input pin hold time	Thold			20		ns
Output pin delay time	Tdelay	Cload=20pF		50		ns

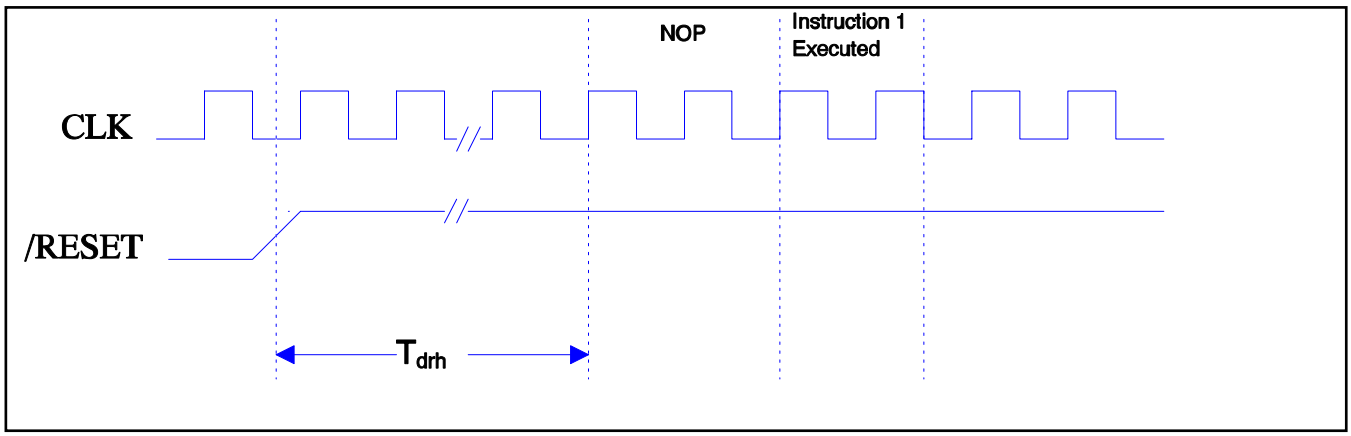
Note : N= selected prescaler ratio.

AC Test Input/Output Waveform

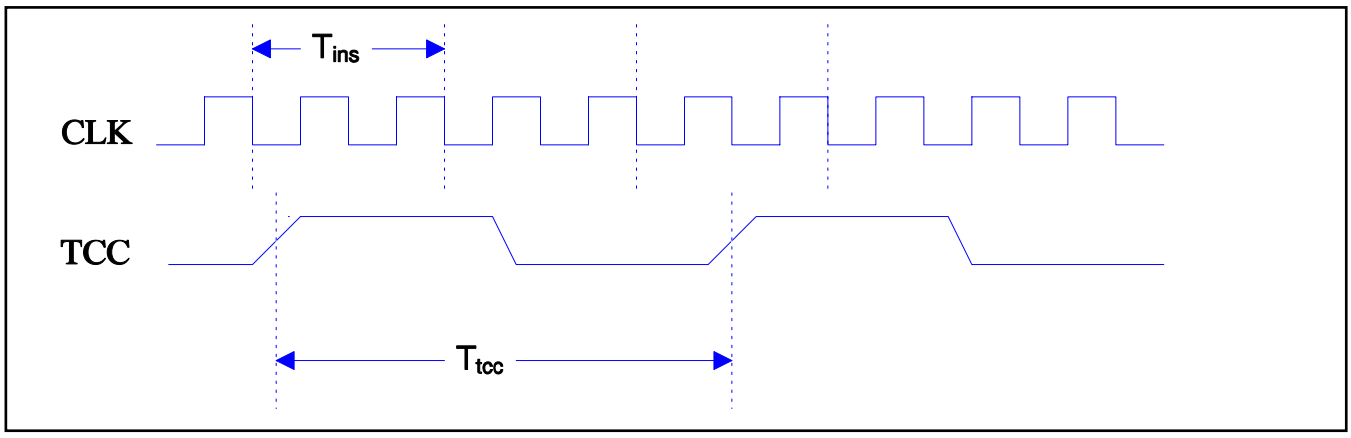


AC Testing: Input are driven at 2.4V for logic "1", and 0.45V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

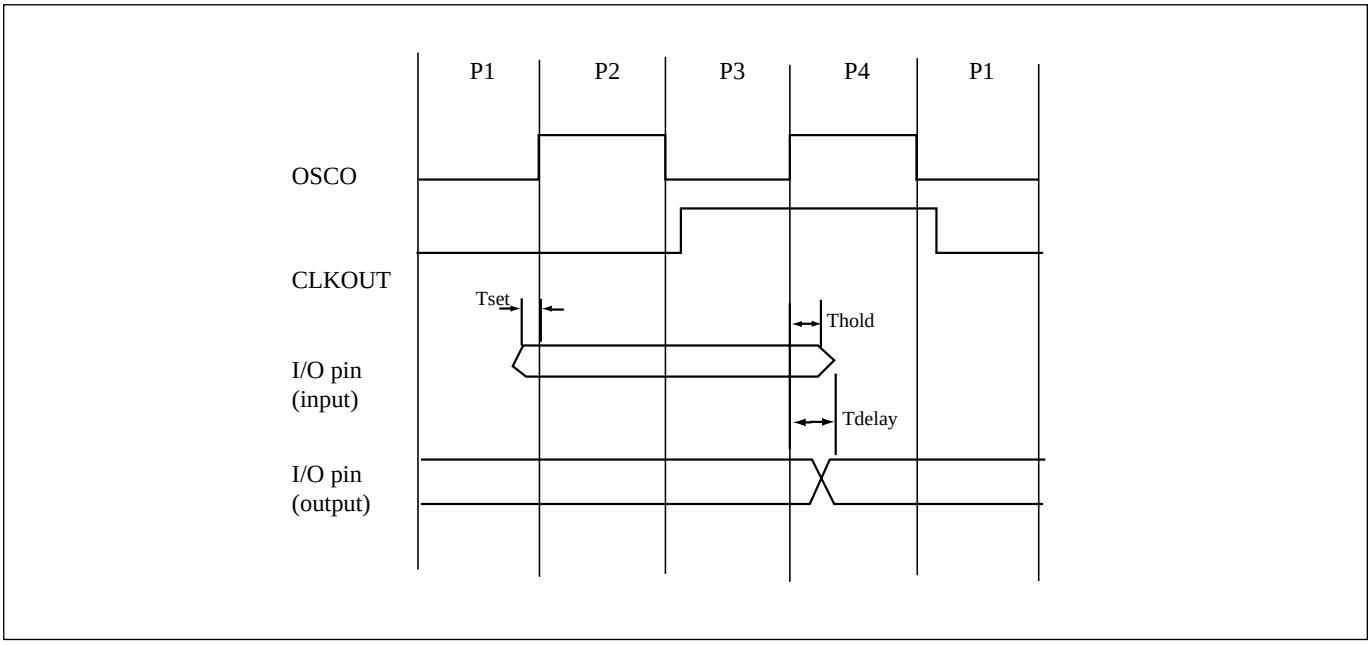
RESET Timing (CLKS="0")



TCC Input Timing (CLKS="0")



I/O PIN TIMING (CLKS="0")



Notes : CLKOUT is available only in RC oscillator mode.